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EXAMINER	
TSEGAYE, SABA	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/732,497	BECHTOLSHEIM ET AL.	
	Examiner	Art Unit	
	Saba Tsegaye	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,23-33,35,37,38 and 40-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 23-33, 35, 37, 38, and 40-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to the amendment filed 08/14/06. Claims 1-18, 23-33, 35, 37, 38, and 40-43 are pending. Currently no claims are in condition for allowance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 23-33, 35, 37, 38, and 40-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 23, line 1, the phrase "the computer-implemented steps" lacks antecedent basis.

Claim Rejections - 35 USC § 102

4. Claims 23, 25-29, 31-33, 37, 38 and 40-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffman et al. (US 6,094,435).

Regarding claim 23, Hoffman discloses, in Figs. 3-4, a method for packet processing comprising the computer-implemented steps of:

at a Packet Processing Engine (50i), receiving a plurality of input packets at one or more input interfaces (38i), distinguishing first packet header information from a first input packet (once input port 50i buffered received packet, the input port 50i passes **the header** to the forwarding logic 52), and forwarding said first packet header information to a Fast Forwarding

Engine (the input port 50i passes **the header** to the forwarding logic 52 (column 9, lines 19-25; column 15, lines 55-65));

at the Fast Forwarding Engine (52), determining packet forwarding information (column 9, line 27-column 10, line 3), and sending said packet forwarding information to the Packet Processing Engine (after the forwarding logic 52 has determined what to do with the packet, it passes that information to the input port 50i);

a network flow routing engine (32) coupled to the Fast Forwarding Engine (52), wherein the network flow routing engine (32) determines network flow packet forwarding information in response to receiving network flow information associated with the first packet header information and provides the network packet forwarding information to the Fast Forwarding Engine, wherein the Fast Forwarding Engine (52) uses the network flow packet forwarding information in generating the packet forwarding information (*forwarding logic 52 uses information which has been placed by the processor 32 into the forwarding memory 40 and associated memory 42*) (column 13, lines 35-50; column 14, lines 51-55; column 22, lines 8-22, and lines 35-50);

generating, at said Packet Processing Engine, an output packet based on said packet forwarding information and said first packet (the input 50i make modifications to the packet as instructed to do so from the forwarding logic 52); and

sending said output packet from a first output interface among one or more output interfaces of the Packet Processing Engine (column 10, lines 14-38),

wherein the Fast Forwarding Engine is coupled to and accesses a forwarding memory (CAM 40 and associated memory 42; see column 9, lines 39-43) to record one or more

forwarding information rules as the forwarding information rules become available to the Fast Forwarding Engine in response to changes in any on of network topology access control, and administrative and managerial rules (different information entries are updated by the forwarding logic 52: such as information relating to source and destination aging; entry information whether a new tag should be applied to an outgoing packet; entry that allows for more than one port to be specified (multicast addressing); entry that includes a priority for the packet etc. see column 16, line 3-column 17, line 9; column 17, lines 36-40; see fig. 4).

Regarding claim 25, Hoffman discloses a method, wherein said one or more input interfaces are coupled to at least one communication network (see figure 1, LAN 28 and network 14).

Regarding claim 26, Hoffman discloses a method, wherein the step of distinguishing first packet header information from a first input packet is performed by parsing said first packet (arriving packets are stored in the packet memory 50i and the input port 50i passes the header to the forwarding logic 52; further, Hoffman discloses that software running on the router parses an incoming packet (see column 7, lines 49-50; column 8, lines 26-28).

Regarding claim 27, Hoffman discloses a method, wherein the packets are stored and accessed by a packet index (column 18, lines 35-39).

Regarding claim 28 Hoffman discloses a method, wherein the first packet header includes an IP source address, IP source port P destination address, IP destination port, protocol type, and information indicating whether the packet is unicast or multicast (packets using the TCP/IP protocol have been received at the input port and it is part of this standard to have the source, destination, protocol type and information indicating whether the packet is unicast or multicast of the packet included in each packet to allow for proper routing (column 16, lines 3-30)).

Regarding claim 29, Hoffman discloses a method wherein the step of generating an output packet based on said packet forwarding information includes a rewrite operation (column 10, lines 14-16).

Regarding claim 31, Hoffman discloses a method wherein said Fast Forwarding Engine is coupled to assistance devices for assisting in making packet-forwarding decisions (see figure 4; 32, 40, 42).

Regarding claim 32, Hoffman discloses a method wherein said Fast Forwarding Engine is coupled to a set of routing information memories (column 8, lines 56-61; column16, lines 23-36).

Regarding claim 33, Hoffman discloses a method wherein said Fast Forwarding Engine is coupled to a forwarding content addressable memory (CAM 40; see figure 4).

Regarding claim 37, Hoffman discloses a method wherein the Fast Forwarding Engine sends the packet header information to the forwarding Content Addressable Memory (column 9, lines 37-47).

Regarding claim 38, Hoffman discloses a method wherein the Content Addressable Memory determines packet-forwarding information based on the packet header information (column 9, lines 37-47).

Regarding claim 40, Hoffman discloses a method wherein the Fast Forwarding Engine accesses the forwarding Content Addressable Memory to retrieve the packet forwarding information (column 9, lines 39-47).

Regarding claim 41, Hoffman discloses a method wherein the Fast Forwarding Engine forwards an identifier to said first input interface to determine if access is permitted for said first packet (column 15, lines 55-65).

Regarding claim 42, Hoffman discloses a method wherein the Fast Forwarding Engine forwards an identifier to said first output interface to determine if access is permitted for said first packet (column 15, lines 55-65).

Regarding claim 43, Hoffman discloses a method further comprising the step of storing said first packet in said Packet Processing Engine (port 50i has buffered at least the first 64 bytes of the received packet).

Claim Rejections - 35 USC § 103

5. Claims 1-3, 7-16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. in view of Carvey et al. (US 6,359,879).

Regarding claim 1, Hoffman discloses, in Figs. 1-4, Apparatus including:

a first device (50i) having a plurality of network input interfaces (38i) and a plurality of network output interfaces (38i), said first device including a packet information extractor (50i; column 9, lines 23-26) coupled to at least one of said network input interface (38i), said first device comprising logic for extraction packet information without performing packet forwarding decisions (column 9, lines 23-26);

a second device (52) coupled to said packet information extractor (50i), said second device capable of generating packet forwarding information and output port information responsive to an output of said packet information extractor (column 9, lines 27-47), wherein the second device access a forwarding memory (CAM 40; see column 9, lines 39-43) to record one or more forwarding information rules as the forwarding information rules become available to the second device in response to changes in any one of network topology, access control, and administrative and managerial rules (different information entries are updated by the forwarding logic 52: such as information relating to source and destination aging; entry information whether a new tag should be applied to an outgoing packet; entry that allows for more than one port to be

specified (multicast addressing); entry that includes a priority for the packet etc. see column 16, line 3-column 17, line 9; column 17, lines 36-40; see fig. 4);

an information link, coupled to the first device and said second device (column 9, lines 23-26; see figure 3);

a network flow routing engine (32) coupled to the second device (52), wherein the network flow routing engine (32) determines network flow packet forwarding information in response to receiving network flow information associated with the output of the packet information extractor and provides the network flow packet forwarding information to the second device, wherein the second device uses the network flow packet forwarding information in generating the packet forwarding information (*forwarding logic 52 uses information which has been placed by the processor 32 into the forwarding memory 40 and associated memory 42*) (column 13, lines 35-50; column 14, lines 51-55; column 22, lines 8-22, and lines 35-50). As is well known in the art, parallel processing is a method of processing that contains two or more processor running simultaneously. Furthermore, Hoffman discloses that processing by the class logic 60, the L2 logic 62, and L3 logic 64 may proceed in a parallel or pipelined fashion (column 17, line 66-column 18, line1).

Hoffman does not expressly discloses: wherein said second device performs generating packet forwarding information substantially for first packets substantially in parallel with said first device performing extracting packet information for other packets.

Carvey teaches, in fig. 8, a router that performs a process of forwarding an incoming packet. A header is extracted at a first device 301, and a second device 305, 307 is used to look up the output trunk in a routing table (fast forwarding engine). Fig. 7 shows a flow chart of the

process of forwarding of an incoming packet. The forwarding process of fig. 7 is pipelined as shown in fig. 8. By pipelining the process, the router is able to process packets with a very high throughput by operating on several packets simultaneously (column 5, lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a parallel processing, such as that suggested by Carvey, to the method of Hoffman. One of ordinary skill in the art would have been motivated to do this because using parallel processing allows to process packets with a very high throughput by operating on several packets simultaneously.

Regarding claim 2, Hoffman discloses the apparatus wherein the first device includes a packet rewriter coupled to at least one the network output interface (column 10, lines 14-48); and

the second device includes a packet rewrite generator coupled to the first device, the packet rewrite generator disposed for generating the packet forwarding in formation and output port information (column 10, lines 14-61);

wherein the packet rewrite element is responsive to the packet rewrite generator (column10, lines 15-61).

Regarding claim 3, Hoffman discloses the apparatus including a packet buffer memory (44) coupled to the first device (column 9, lines 62-66).

Regarding claims 7-9, Hoffman discloses a rewrite table and address pointing to the rewrite table (column 10, lines 14-39).

Regarding claim 10, Hoffman discloses an apparatus including; a first device (50i) having at least one input interface (38i) and at least one output interface (38i, 56), the first device including an intonation extractor (50i) having an input coupled to a packet received from the input interface and having an output coupled to a first memory (44), the first device comprising logic for extracting packet information without performing packet forwarding decisions; and

a second device (52) including a decision generator having an input coupled to the first device (50i, column 12, lines 7-12) and having an output coupled to the first device (50i; column 12, lines 12-16); wherein the first device is responsive to a forwarding treatment from the second device to determine a set of the output interfaces on which to couple the packet (column 10, lines 4-48), wherein the second device accesses a forwarding memory (CAM 40; see column 9, lines 39-43) to record one or more forwarding information rules as the forwarding information rules become available to the second device in response to changes in any one of network topology, access control, and administrative and managerial rules (different information entries are updated by the forwarding logic 52: such as information relating to source and destination aging; entry information whether a new tag should be applied to an outgoing packet; entry that allows for more than one port to be specified (multicast addressing); entry that includes a priority for the packet etc. see column 16, line 3-column 17, line 9; column 17, lines 36-40; see fig. 4);

a network flow routing engine (32) coupled to the second device (52), wherein the network flow routing engine (32) determines network flow packet forwarding information in response to receiving network flow information associated with the packet information extracted by the information extractor and provides the network flow packet forwarding information to the second device, wherein the second device uses the network flow packet forwarding information

in generating the packet forwarding information (*forwarding logic 52 uses information which has been placed by the processor 32 into the forwarding memory 40 and associated memory 42*) (column 13, lines 35-50; column 14, lines 51-55; column 22, lines 8-22, and lines 35-50). As is well known in the art, parallel processing is a method of processing that contains two or more processor running simultaneously. Furthermore, Hoffman discloses that processing by the class logic 60, the L2 logic 62, and L3 logic 64 may proceed in a parallel or pipelined fashion (column 17, line 66-column 18, line1).

Hoffman does not expressly discloses: wherein said second device performs generating packet forwarding information substantially for first packets substantially in parallel with said first device performing extracting packet information for other packets.

Carvey teaches, in fig. 8, a router that performs a process of forwarding an incoming packet. A header is extracted at a first device 301, and a second device 305, 307 is used to look up the output trunk in a routing table (fast forwarding engine). Fig. 7 shows a flow chart of the process of forwarding of an incoming packet. The forwarding process of fig. 7 is pipelined as shown in fig. 8. By pipelining the process, the router is able to process packets with a very high throughput by operating on several packets simultaneously (column 5, lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a parallel processing, such as that suggested by Carvey, to the method of Hoffman. One of ordinary skill in the art would have been motivated to do this because using parallel processing allows to process packets with a very high throughput by operating on several packets simultaneously.

Regarding claim 11, Hoffman discloses the apparatus wherein the first device includes a packet rewriter coupled to at least one the network output interface (column 10, lines 14-48); and

the second device includes a packet rewrite generator coupled to the first device, the packet rewrite generator disposed for generating the packet forwarding in formation and output port information (column 10, lines 14-61);

wherein the packet rewrite element is responsive to the packet rewrite generator (column10, lines 15-61).

Regarding claim 12, Hoffman discloses the apparatus wherein the forwarding treatment includes at least one action relating to accounting (column 22, lines 23-34).

Regarding claim 14, Hoffman discloses the apparatus wherein the forwarding treatment is responsive to information regarding class of service or quality of service (column 12, lines 56-67).

Regarding claim 15, Hoffman discloses that the multiplayer network element 12 combines the functions of both a bridge and a router (column 8, lines 26-37). Software running on the router is responsive to information regarding parsing, extracting and encoding the packet information (column 7, line 49-column 8, line 11; column 14, lines 4-1 1).

Regarding claims 13 and 16, Hoffman discloses the apparatus wherein the forwarding treatment is responsive to the packet information memory (column 10, lines 4-48).

Regarding claim 24, Hoffman discloses all the claim limitations as stated in claim 23. Furthermore, Hoffman discloses that processing by the class logic 60, the L2 logic 62, and L3 logic 64 may proceed in a parallel or pipelined fashion (column 17, line 66-column 18, line1).

Hoffman does not expressly disclose that the packet processing engine and the steps performed by the fast forwarding engine are performed in parallel.

Carvey teaches, in fig. 8, a router that performs a process of forwarding an incoming packet. A header is extracted at a first device 301, and a second device 305, 307 is used to look up the output trunk in a routing table (fast forwarding engine). Fig. 7 shows a flow chart of the process of forwarding of an incoming packet. The forwarding process of fig. 7 is pipelined as shown in fig. 8. By pipelining the process, the router is able to process packets with a very high throughput by operating on several packets simultaneously (column 5, lines 50-53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add a parallel processing, such as that suggested by Carvey, to the method of Hoffman. One of ordinary skill in the art would have been motivated to do this because using parallel processing allows to process packets with a very high throughput by operating on several packets simultaneously.

6. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. in view of Kerr et al. (US 6,513,108)

Hoffman discloses all the claim limitations as stated above. Further, Hoffman discloses that packets are modified before forwarding the packets to appropriate output ports. Hoffman, further, discloses that the entry in the associated memory 42 may include the next hop

destination address to be used to replace the incoming destination in unicast routing. However, Hoffman does not expressly disclose that the rewrite operation includes adjusting hop count for the packet, determining a new CRC and performing packet-reformatting operations.

Kerr teaches that processing engine processes the header information and returns a modified header, which includes the address of the next hop station in the network along with additional control information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the teachings or Kerr of include adjusting hop count to the header modification of Hoffman. One of ordinary skill in the art would have been motivated to do this because adjusting hop count would increase packet transfer speed of intermediate nodes.

7. Claims 4-6, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. in view of Carvey et al. as applied to claims 1 and 10 above, and further in view of Freitag, Jr. (US 6,237,054).

Hoffman in view of Carvey discloses all the claim limitations as stated above. Further, Hoffman discloses that the multiplayer network element 12 combines the functions of both a bridge and a router (column 8, lines 26-37). Fig. 4 shows block diagrams of input port 50i (first device) and forwarding logic 52 (second device). Carvey, in fig. 8, shows block diagrams of first device and second device. However, Hoffman in view of Carvey does not expressly disclose a single monolithic semiconductor circuit.

Freitag, Jr. teaches a micro-controller (an integrated circuit) which incorporates a processor core along with one or more support circuits on the same monolithic semiconductor

substrate. The support circuits perform support functions such as communication functions and memory interface functions.

It would have been obvious to one ordinary skill in the art at the time the invention was made to substitute a single monolithic semiconductor, such as that suggested by Freitag, to the multi-layer network element of Hoffman. One of ordinary skill in the art would have been motivated to do this because a single monolithic semiconductor provides lower fabrication costs and higher reliabilities (column 2, lines 43-48).

Allowable Subject Matter

8. Claim 35 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-18, 23-33, 35, 37, 38, and 40-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (571) 272-3091. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ST
August 31, 2006

CHI PHAM
SUPERVISORY PATENT EXAMINER 9/1/06